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Amendments to the Claims

1. (*Currently Amended*) A current mode pipelined analogue-to-digital converter (ADC) comprising a plurality of serially connected conversion stages (S_i) wherein at least one conversion stage comprises, a stage input for receiving a current (r_{i-1}) for conversion, a sample-and-hold (S/H) circuit ~~(120, 130,135)~~ coupled to sample the current at the stage input during a first time period and to hold the sampled current during a second time period, the S/H circuit having first and second outputs ~~(132, 131)~~, the first output ~~(132)~~ delivering a mirror of the sampled current during the first time period and a mirror of the held current during the second time period and the second output ~~(131)~~ delivering the held current directly during the second time period, a current comparator means ~~(140)~~ having an input coupled to the first output of the S/H circuit for comparing a current at said input with one or more reference currents, a digital output coupled to an output of the current comparator means for producing a digital signal *(D)* representing the digital conversion performed by the stage, a digital-to-analogue converter (DAC) ~~(150)~~ having an input coupled to the output of the current comparator means, and a summing means ~~(160)~~ having a first input coupled to an output of the DAC, a second input coupled to the second output of the S/H circuit, and an output for delivering a residual current *(r_i)* during the second time period.

2. (*Currently Amended*) An ADC as claimed in claim 1, wherein the S/H circuit comprises a plurality of first outputs ~~(132, 232)~~ each delivering a mirror of the sampled current during the first time period and a mirror of the held current during the second time period, and further comprising a plurality of current comparator means ~~(140, "140)~~ each having an input coupled to a respective one of the first outputs of the S/H circuit for comparing a current at said input with one or more respective reference currents, and wherein the digital output is coupled to an output of each of the current comparator means for producing a digital signal *(D_p, D_q)* representing the digital conversion performed by the stage, and wherein the DAC has a plurality of inputs each of said inputs respectively coupled to the output of a respective one of the current comparator means.

3. (*Currently Amended*) An ADC as ~~claimed in claim 1 or 2,~~ as claimed in claim 1, wherein the operations during the first and second time periods are interchanged for adjacent conversion stages.

4. (*Currently Amended*) An ADC as claimed in claim 3, comprising two or more pluralities of serially interconnected conversion stages *(S'_i, S_i'')* operating in parallel wherein the operations during the first and second time periods are multiplexed for corresponding parallel conversion stages.

5. (*Currently Amended*) An ADC as ~~claimed in claim 1, 2, 3 or 4,~~ as claimed in claim 1, wherein the current comparator means (140) comprises a non-regenerative circuit (140′).

6. (*Currently Amended*) An ADC as ~~claimed in claim 1 2, 3, or 4,~~ as claimed in claim 1, wherein the current comparator (140) means comprises a regenerative circuit (141).

7. (*Currently Amended*) An electronic device comprising a current mode pipelined analogue-to-digital converter as ~~claimed in any one of claims 1-6.~~ as claimed in claim 1.

8. (*Currently Amended*) An electronic device as claimed in claim 7, wherein the electronic device is a wireless receiver or transceiver.